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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,431	04/02/2007	Haruo Suenaga	41339	8733

52054 7590 07/09/2009
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EXAMINER	
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ART UNIT	**PAPER NUMBER**
3742	

NOTIFICATION DATE	DELIVERY MODE
07/09/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	**Application No.** 10/599,431	**Applicant(s)** SUENAGA ET AL.	
	Examiner THIEN TRAN	**Art Unit** 3742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _28 September 2006_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-9,13,14 and 16-31_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _1-9,13,14 and 16-31_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _02 April 2007_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _9/28/2006 & 6/7/2007_.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 17, 18, 20, 21 are objected to because they are dependent upon claims that have been cancelled. For examining purposes, the examiner interprets that claims 17, 18, 20 and 21 are dependent upon claim 2. Appropriated correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 13 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Bessyo (US Patent 6,362,463).

4. Regarding claim 1, Bessyo teaches a high-frequency heating apparatus for driving a magnetron (Col 5, Lines 66-67), comprising: a DC power supply (Fig 1, Item 31, Col 7, Line 57) including an AC power supply (Fig 7, AC Source, Col 11, Lines 7-10) a rectifier circuit (Fig 1, Item 40, Col 7, Line 56) for rectifying a voltage of the AC power supply, and a smoothing capacitor (Fig 1, Item 43, Col 9, Lines 55-56) for smoothing an output voltage of the rectifier circuit (Fig 1, Item 35, Col 11, Lines 35-40); a series circuit including two semiconductor switching devices (Fig 1, Items 36 & 37, Col 7, Lines 60-63), the series circuit

being connected in parallel to the AC power supply (Fig 1, Items 36 & 37 are connected in parallel to Item 31); a resonance circuit (Fig 1, Items 34 & 35, Col 9, Lines 5-20) connected to a primary winding (Fig 1, Item 33, Col 7, Line 60) of a leakage transformer and a capacitor (Fig 1, Item 32, Col 7, Line 60), one end of the resonance circuit being connected to a middle point of the series circuit (Fig 1, Item 34 is connected between Items 36 and 37) in an AC equivalent circuit while the other end of the resonance circuit is connected to one end of the AC power supply (Fig 1, Item 34 is connected to positive terminal of Item 31, DC power supply includes AC power supply Col 11, Line 7-10); a drive unit (Fig 1, Item 38, Col 8, Line 20) for driving each of the semiconductor switching devices; a rectifier unit (Fig 1, Item 40, Col 7, Line 56) connected to a secondary winding (Fig 1, Item 39, Col 8, Line 1) of the leakage transformer; a magnetron (Fig 1, Item 41, Col 7, Line 57) connected to the rectifier unit (Fig 1, Item 41 is connected to Item 40); and a dead time generation circuit (Fig 1, Items 34-37) for turning off the semiconductor switching devices concurrently (Fig 4a & 4c, Items 36 & 37), wherein the drive unit has a function of limiting the lowest frequency of a frequency with which the semiconductor switching devices are driven (Col 13, Lines 5-7), so that the lowest frequency is set to be high at the beginning of operation of the high-frequency heating apparatus, and the lowest frequency is set to be lower gradually thereafter (Fig 15, Item C, Col 14, Lines 20-25 & Col 12, Lines 57-64, Operating frequency is 30 kHz an is then lowered). Examiner interprets that Bessyo teaches a variable dead time preparation circuit because in Fig 4a & 4c, in modes 2 & 5, the first (Item 36) and second (Item 37)

switching devices are simultaneously turned off (Current = 0) in response to the switching frequency.

5. Regarding claim 3, Bessyo teaches a high-frequency heating apparatus for driving a magnetron (Col 5, Lines 66-67), comprising: a DC power supply (Fig 1, Item 31, Col 7, Line 57) including an AC power supply (Fig 7, AC Source, Col 11, Lines 7-10) a rectifier circuit (Fig 1, Item 40, Col 7, Line 56) for rectifying a voltage of the AC power supply, and a smoothing capacitor (Fig 1, Item 43, Col 9, Lines 55-56)for smoothing an output voltage of the rectifier circuit (Fig 1, Item 35, Col 11, Lines 35-40); a series circuit including two semiconductor switching devices (Fig 1, Items 36 & 37, Col 7, Lines 60-63), the series circuit being connected in parallel to the AC power supply (Fig 1, Items 36 & 37 are connected in parallel to Item 31); a resonance circuit (Fig 1, Items 34 & 35, Col 9, Lines 5-20) connected to a primary winding (Fig 1, Item 33, Col 7, Line 60) of a leakage transformer and a capacitor (Fig 1, Item 32, Col 7, Line 60), the resonance circuit being connected in parallel to one of the semiconductor switching devices (Items 34 & 35 are connected in parallel to Item 37); a drive unit (Fig 1, Item 38, Col 8, Line 20) for driving each of the semiconductor switching devices; a rectifier unit (Fig 1, Item 40, Col 7, Line 56) connected to a secondary winding (Fig 1, Item 39, Col 8, Line 1) of the leakage transformer; a magnetron (Fig 1, Item 41, Col 7, Line 57) connected to the rectifier unit (Fig 1, Item 41 is connected to Item 40); and a dead time generation circuit (Fig 1, Items 34-37) for turning off the semiconductor switching devices concurrently (Fig 4a & 4c, Items 36 & 37), wherein the drive unit has a function of limiting the

lowest frequency of a frequency with which the semiconductor switching devices are driven (Col 13, Lines 5-7), so that the lowest frequency is set to be high at the beginning of operation of the high-frequency heating apparatus, and the lowest frequency is set to be lower gradually thereafter (Fig 15, Item C, Col 14, Lines 20-25 & Col 12, Lines 57-64, Operating frequency is 30 kHz an is then lowered). Examiner interprets that Bessyo teaches a variable dead time preparation circuit because in Fig 4a & 4c, in modes 2 & 5, the first (Item 36) and second (Item 37) switching devices are simultaneously turned off (Current = 0) in response to the switching frequency.

6. Regarding claims 13 and 30, as applied to claims 1 and 3, Bessyo teaches where the dead time generation circuit (Fig 1, Items 34-37) generates a dead time based on positive and negative offset voltages (Fig 4b & 4d, Items 3 & 37) each varying with a first inclination in proportion to increase of a switching frequency and varying with a second inclination when the switching frequency reaches a predetermined frequency or higher.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 2, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) in view of Manabu (Japan Patent Publication 2003-259643). An English-language equivalent has been adopted for Japanese reference Manabu (Japan Patent Publication 2003-259643) and is included in PTO-892 Notice of Reference Cited.

10. Regarding claim 2, Bessyo teaches a high-frequency heating apparatus for driving a magnetron (Col 5, Lines 66-67), comprising: a DC power supply (Fig 1, Item 31, Col 7, Line 57) including an AC power supply (Fig 7, AC Source, Col 11, Lines 7-10) a rectifier circuit (Fig 1, Item 40, Col 7, Line 56) for rectifying a voltage of the AC power supply, and a smoothing capacitor (Fig 1, Item 43, Col 9, Lines 55-56) for smoothing an output voltage of the rectifier circuit (Fig 1, Item 35, Col 11, Lines 35-40); a resonance circuit (Fig 1, Items 34 & 35, Col 9, Lines 5-20) connected to a primary winding (Fig 1, Item 33, Col 7, Line 60) of a leakage transformer and a capacitor (Fig 1, Item 32, Col 7, Line 60), a drive unit (Fig 1, Item 38, Col 8, Line 20) for driving each of the semiconductor switching devices; a rectifier unit (Fig 1, Item 40, Col 7, Line 56) connected to a secondary

winding (Fig 1, Item 39, Col 8, Line 1) of the leakage transformer; a magnetron (Fig 1, Item 41, Col 7, Line 57) connected to the rectifier unit (Fig 1, Item 41 is connected to Item 40); and a dead time generation circuit (Fig 1, Items 34-37) for turning off the semiconductor switching devices concurrently, wherein the drive unit has a function of limiting the lowest frequency of a frequency with which the semiconductor switching devices are driven (Col 13, Lines 5-7), so that the lowest frequency is set to be high at the beginning of operation of the high-frequency heating apparatus, and the lowest frequency is set to be lower gradually thereafter (Fig 15, Item C, Col 14, Lines 20-25 & Col 12, Lines 57-64, Operating frequency is 30 kHz an is then lowered). Examiner interprets that Bessyo teaches a variable dead time preparation circuit because in Fig 4a & 4c, in modes 2 & 5, the first (Item 36) and second (Item 37) switching devices are simultaneously turned off (Current = 0) in response to the switching frequency. Bessyo does not teach two series circuits each including two semiconductor switching devices, each of the series circuits being connected in parallel to the AC power supply; one end of the resonance circuit being connected to a middle point of one of the series circuits while the other end of the resonance circuit is connected to a middle point of the other series circuit.

11. In analogous art of current resonance type soft switching power circuit, Manabu discloses two series circuits including two semiconductor switching devices (Drawing 1, Q1 & Q2 is the first series circuit, Q3 & Q4 is the second series circuit, Pg 20, Description of Notations), each of the series circuits being connected in parallel to the AC power supply (Drawing 1, First Series (Q1 & Q2)

and Second Series (Q3 & Q4) are in parallel with Item E, Pg 20, Description of Notations); one end of the resonance circuit being connected to a middle point of one of the series circuits (Drawing 1, Item 2, Rectification Circuit is connected between Q1 & Q2) while the other end of the resonance circuit is connected to a middle point of the other series circuit (Drawing 1, Item 2, Rectification Circuit is connected between Q2 & Q3) for the benefit of providing soft switching in a current resonance type soft switching power circuit (Abstract, Pg 2, Lines 1-3). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Manabu for the benefit of providing soft switching in a current resonance type soft switching power circuit.

12. Regarding claim 20, as applied to claim 2, Bessyo does not teach where the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency. In analogous art of current resonance type soft switching power circuit, Manabu discloses where the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency (Pg 13, 0028, Lines 15-17) for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output (Pg 13, 0028, Lines 16-17). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Manabu for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output.

13. Regarding claim 22, as applied to claim 2, Bessyo teaches where the dead time generation circuit (Fig 1, Items 34-37) generates a dead time based on positive and negative offset voltages (Fig 4b & 4d, Items 3 & 37) each varying with a first inclination in proportion to increase of a switching frequency and varying with a second inclination when the switching frequency reaches a predetermined frequency or higher.

14. Claims 4, 5, 6 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) as applied to claims 1 and 3, in view of Noda (US Patent 5,274,208).

15. Regarding claims 4 and 24, Bessyo teaches where frequency of the lowest frequency limiting circuit is set to be higher than the output of the frequency-modulated signal generation circuit at the beginning of operation of the aforementioned high-frequency heating apparatus, and in accordance with time having passed since the beginning of operation, the limited frequency is lowered gradually, while with lowering of the limited frequency, a signal higher in switching frequency of the limited frequency and the output signal of the frequency-modulated signal generation circuit is selected as a signal to be supplied to the dead time generation circuit (Fig 1, Items 34-37) in accordance with time having passed, so that the selected signal is changed over gradually to the output signal of the frequency-modulated signal generation circuit (Fig 15, Item C, Col 14, Lines 20-25 & Col 12, Lines 57-64, Operating frequency is 30 kHz and is then lowered). Bessyo does not teach an error signal generation

circuit for generating an error signal from a difference between an input current of the AC power supply and a reference current; and a frequency-modulated signal generation circuit for correcting a rectified voltage/rectified current obtained by rectifying the AC power supply, based on an output (error signal) of the error signal generation circuit, an output of the frequency-modulated signal generation circuit being supplied to the dead time generation circuit; wherein a lowest frequency limiting circuit is inserted between the frequency-modulated signal generation circuit and the dead time generation circuit, the lowest frequency limiting circuit supplies a limited frequency to the dead time generation circuit based on the output signal of the frequency-modulated signal generation circuit.

16. In analogous art of high frequency heating apparatus, Noda discloses an error signal generation circuit (Fig 2, Item 26, Col 6, Line 44) for generating an error signal from a difference between an input current of the AC power supply and a reference current (Col 6, Lines 39-44); and a frequency-modulated signal generation circuit (Fig 2, Item 27, Col 6, Lines 45-49) for correcting a rectified voltage/rectified current (Fig 2, Item 25, Col 6, Lines 39-42) obtained by rectifying the AC power supply, based on an output (error signal) of the error signal generation circuit, an output of the frequency-modulated signal generation circuit (Fig 2, Item S3, Col 6, Lines 50-54) being supplied to the dead time generation circuit; wherein a lowest frequency limiting circuit (Fig 2, Item 34, Col 7, Lines 13-15) is inserted between the frequency-modulated signal generation circuit and the dead time generation circuit, the lowest frequency limiting circuit

supplies a limited frequency (Fig 2, Item S5, Col 7, Line 14-15) to the dead time generation circuit based on the output signal of the frequency-modulated signal generation circuit for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied (Col 1, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Noda for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied.

17. Regarding claim 5, as applied to claims 1 and 4, Bessyo does not teach where the lowest frequency limiting circuit has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied to the dead time generation circuit, and charges accumulated in the capacitor are discharged. In analogous art of high frequency heating apparatus, Noda discloses where the lowest frequency limiting circuit (Fig 2, Item 34, Col 7, Lines 13-15) has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied (Fig 2, Item Vmax, Col 7, Lines 10-15), to the dead time generation circuit and charges accumulated in the capacitor are discharged (Fig 2, Item S5, Col 7, Lines 12-18) for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply

voltages are supplied (Col 1, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Noda for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied. Examiner interprets that it is well known in the art that the overvoltage detection circuit of Noda has a capacitor for generating signal S5 (Fig 2, Item S5, Col 7, Lines 12-18).

18. Regarding claim 6, as applied to claim 1 and 4, the applicant discloses that the dead time generation circuit generates a fixed or marginally increased dead time regardless of a switching frequency as being well known in the art (Specification, Pg 29, Lines 1-2).

19. Claims 7, 9 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) as applied to claims 1 and 3, in view of Teruya (Japan Patent Publication 2003-257604). An English-language equivalent has been adopted for Japanese reference Teruya (Japan Patent Publication 2003-257604) and is included in PTO-892 Notice of Reference Cited.

20. Regarding claims 7 and 27, Bessyo does not teach where the dead time generation circuit generates a dead time increased in accordance with increase of a switching frequency. In analogous art of inverter cooker, Teruya discloses where the dead time generation circuit generates a dead time increased in accordance with increase of a switching frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously

variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

21. Regarding claim 9, as applied to claims 1 and 7, Bessyo does not teach where the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency. In analogous art of inverter cooker, Teruya discloses where the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

22. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) in view of Teruya (Japan Patent Publication 2003-257604) as applied to claims 1 and 7 and further in view of Manabu (Japan Patent Publication 2003-259643). An English-language equivalent has

been adopted for Japanese reference Teruya (Japan Patent Publication 2003-257604) and Manabu (Japan Patent Publication 2003-259643) and is included in PTO-892 Notice of Reference Cited.

23. Regarding claim 8, Bessyo in view of Teruya does not teach where the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency. In analogous art of current resonance type soft switching power circuit, Manabu discloses where the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency (Pg 13, 0028, Lines 15-17) for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output (Pg 13, 0028, Lines 16-17). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and Teruya with the disclosure of Manabu for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output.

24. Claims 14 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) as applied to claims 1 and 3, in view of Yang (US Patent Publication 2005/0174819).

25. Regarding claim 14 and 31, Bessyo teaches where the dead time generation circuit includes a first current varying in proportion to a switching frequency (Fig 4, Item a), a second current beginning to flow at a predetermined frequency and varying in proportion to the switching frequency (Fig 3, Item c). Bessyo does not teach where the dead time generation circuit includes a third

current obtaining by and multiplying a combining current of the two currents by a predetermined coefficient, and a upper and lower potential generation unit for generating two upper and lower potentials obtained by adding positive and negative offset voltages proportional to the third current, to the duty control power supply respectively, and a dead time is generated based on the two upper and lower potentials. In analogous art of synchronous rectification circuit with dead time regulation, Yang discloses where the dead time generation circuit includes a VCC power supply (Pg 2, 0022), a duty control power supply (Pg 2, 0022), a third current obtaining by and multiplying a combining current of the two currents by a predetermined coefficient and a upper and lower potential generation unit for generating two upper and lower potentials obtained by adding positive and negative offset voltages proportional to the third current, to the duty control power supply respectively, and a dead time is generated based on the two upper and lower potentials (Pg 1, 0014) for the benefit of improving the long dead time and efficiency resulting from an unstable voltage waveform (Pg 1, 0012). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Yang for the benefit of improving the long dead time and efficiency resulting from an unstable voltage waveform.

26. Claims 16, 17, 18, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) in view of Manabu (Japan Patent Publication 2003-259643) as applied to claim 2, further in view of Noda (US Patent 5,274,208).

27. Regarding claim 16, Bessyo in view of Manabu teaches where the frequency of the lowest frequency limiting circuit is set to be higher than the output of the frequency-modulated signal generation circuit at the beginning of operation of the aforementioned high-frequency heating apparatus, and in accordance with time having passed since the beginning of operation, the limited frequency is lowered gradually, while with lowering of the limited frequency, a signal higher in switching frequency of the limited frequency and the output signal of the frequency-modulated signal generation circuit is selected as a signal to be supplied to the dead time generation circuit (Fig 1, Items 34-37) in accordance with time having passed, so that the selected signal is changed over gradually to the output signal of the frequency-modulated signal generation circuit (Fig 15, Item C, Col 14, Lines 20-25 & Col 12, Lines 57-64, Operating frequency is 30 kHz an is then lowered). Bessyo in view of Manabu does not teach an error signal generation circuit for generating an error signal from a difference between an input current of the AC power supply and a reference current; and a frequency-modulated signal generation circuit for correcting a rectified voltage/rectified current obtained by rectifying the AC power supply, based on an output (error signal) of the error signal generation circuit, an output of the frequency-modulated signal generation circuit being supplied to the dead time generation circuit; wherein a lowest frequency limiting circuit is inserted between the frequency-modulated signal generation circuit and the dead time generation circuit, the lowest frequency limiting circuit supplies a

limited frequency to the dead time generation circuit based on the output signal of the frequency-modulated signal generation circuit.

28. In analogous art of high frequency heating apparatus, Noda discloses an error signal generation circuit (Fig 2, Item 26, Col 6, Line 44) for generating an error signal from a difference between an input current of the AC power supply and a reference current (Col 6, Lines 39-44); and a frequency-modulated signal generation circuit (Fig 2, Item 27, Col 6, Lines 45-49) for correcting a rectified voltage/rectified current (Fig 2, Item 25, Col 6, Lines 39-42) obtained by rectifying the AC power supply, based on an output (error signal) of the error signal generation circuit, an output of the frequency-modulated signal generation circuit (Fig 2, Item S3, Col 6, Lines 50-54) being supplied to the dead time generation circuit; wherein a lowest frequency limiting circuit (Fig 2, Item 34, Col 7, Lines 13-15) is inserted between the frequency-modulated signal generation circuit and the dead time generation circuit, the lowest frequency limiting circuit supplies a limited frequency (Fig 2, Item S5, Col 7, Line 14-15) to the dead time generation circuit based on the output signal of the frequency-modulated signal generation circuit for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied (Col 1, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and Manabu with the disclosure of Noda for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied.

29. Regarding claim 17, Bessyo in view of Manabu does not teach where the lowest frequency limiting circuit has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied to the dead time generation circuit, and charges accumulated in the capacitor are discharged. In analogous art of high frequency heating apparatus, Noda discloses where the lowest frequency limiting circuit (Fig 2, Item 34, Col 7, Lines 13-15) has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied (Fig 2, Item Vmax, Col 7, Lines 10-15), to the dead time generation circuit and charges accumulated in the capacitor are discharged (Fig 2, Item S5, Col 7, Lines 12-18) for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied (Col 1, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and Manabu with the disclosure of Noda for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied. Examiner interprets that it is well known in the art that the overvoltage detection circuit of Noda has a capacitor for generating signal S5 (Fig 2, Item S5, Col 7, Lines 12-18).

30. Regarding claim 18, the applicant discloses that the dead time generation circuit generates a fixed or marginally increased dead time regardless of a switching frequency as being known in the art (Specification, Pg 29, Lines 1-2).

31. Regarding claim 25, as applied to claims 2 and 20, Bessyo in view of Manabu does not teach where the lowest frequency limiting circuit has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied to the dead time generation circuit, and charges accumulated in the capacitor are discharged. In analogous art of high frequency heating apparatus, Noda discloses where the lowest frequency limiting circuit (Fig 2, Item 34, Col 7, Lines 13-15) has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied (Fig 2, Item Vmax, Col 7, Lines 10-15), to the dead time generation circuit and charges accumulated in the capacitor are discharged (Fig 2, Item S5, Col 7, Lines 12-18) for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied (Col 1, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and Manabu with the disclosure of Noda for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied. Examiner interprets that it is well known in the art that the overvoltage

detection circuit of Noda has a capacitor for generating signal S5 (Fig 2, Item S5, Col 7, Lines 12-18).

32. Regarding claim 26, as applied to claims 2 and 20, the applicant discloses that the dead time generation circuit generates a fixed or marginally increased dead time regardless of a switching frequency as being well known in the art (Specification, Pg 29, Lines 1-2).

33. Claims 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) in view of Manabu (Japan Patent Publication 2003-259643) as applied to claim 2, further in view of Teruya (Japan Patent Publication 2003-257604).

34. Regarding claim 19, Bessyo in view of Manabu does not teach where the dead time generation circuit generates a dead time increased in accordance with increase of a switching frequency. In analogous art of inverter cooker, Teruya discloses where the dead time generation circuit generates a dead time increased in accordance with increase of a switching frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and Manabu with the disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

35. Regarding claim 21, Bessyo in view of Manabu does not teach where the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency. In analogous art of inverter cooker, Teruya discloses where the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and Manabu with the disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

36. Claims 23 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) in view of Manabu (Japan Patent Publication 2003-259643) as applied to claim 2, further in view of Yang (US Patent Publication 2005/0174819).

37. Regarding claim 23, Bessyo in view of Manabu teaches where the dead time generation circuit includes a first current varying in proportion to a switching frequency (Fig 4, Item a), a second current beginning to flow at a predetermined frequency and varying in proportion to the switching frequency (Fig 3, Item c). Bessyo does not teach where the dead time generation circuit includes a third current obtaining by and multiplying a combining current of the two currents by a

predetermined coefficient, and a upper and lower potential generation unit for generating two upper and lower potentials obtained by adding positive and negative offset voltages proportional to the third current, to the duty control power supply respectively, and a dead time is generated based on the two upper and lower potentials. In analogous art of synchronous rectification circuit with dead time regulation, Yang discloses where the dead time generation circuit includes a VCC power supply (Pg 2, 0022), a duty control power supply (Pg 2, 0022), a third current obtaining by and multiplying a combining current of the two currents by a predetermined coefficient and a upper and lower potential generation unit for generating two upper and lower potentials obtained by adding positive and negative offset voltages proportional to the third current, to the duty control power supply respectively, and a dead time is generated based on the two upper and lower potentials (Pg 1, 0014) for the benefit of improving the long dead time and efficiency resulting from an unstable voltage waveform (Pg 1, 0012). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Yang for the benefit of improving the long dead time and efficiency resulting from an unstable voltage waveform.

38. Regarding claim 28 as applied to claims 2 and 23, Bessyo does not teach where the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency. In analogous art of current resonance type soft switching power circuit, Manabu discloses where the dead time generation circuit fixes or marginally increases

the dead time at a switching frequency not higher than a predetermined frequency (Pg 13, 0028, Lines 15-17) for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output (Pg 13, 0028, Lines 16-17). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Manabu for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output.

39. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) in view of Manabu (Japan Patent Publication 2003-259643) further in view of Yang (US Patent Publication 2005/0174819) as applied to claims 2 and 23, further in view of Teruya (Japan Patent Publication 2003-257604).

40. Regarding claim 29, Bessyo in view of Manabu and further in view of Yang does not teach where the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency. In analogous art of inverter cooker, Teruya discloses where the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, Manabu and Yang with the disclosure of

Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

Double Patenting

41. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

42. Claims 1-3 of this application conflict with claims 1-3 of Application No. 10/571846. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is

required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

43. Claims 1-3 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-3 of copending Application No. 10/571846 (hereafter, '846) in view of Moriya. Moriya discloses a high frequency heating apparatus with a variable dead time preparation circuit that enables the dead time to remain constant at below a predetermined frequency and causes the dead time to increase sharply at a point above a predetermined frequency; knowledge from both references would have allowed one of ordinary skill in the art to arrive at an identical invention. The discussions of Moriya from above is incorporated here by reference.

This is a <u>provisional</u> obviousness-type double patenting rejection.

Application # 10/599431	Application # 10/571846
Claim 1. A high-frequency heating apparatus for driving a magnetron, comprising: DC power supply including an AC power supply, a rectifier circuit for rectifying a voltage of the AC power supply, and a smoothing capacitor for smoothing an output voltage of the rectifier circuit; a series circuit including	Claim 1. A high frequency heating apparatus for driving a magnetron, comprising, a direct current power supply; a series circuit comprising a pair of semiconductor switching elements; and a resonance circuit connected with a primary coil of a leakage transformer and a capacitor;

two semiconductor switching devices, the series circuit being connected in parallel to the AC power supply; a resonance circuit connected to a primary winding of a leakage transformer and a capacitor, one end of the resonance circuit being connected to a middle point of the series circuit in an AC equivalent circuit while the other end of the resonance circuit is connected to one end of the AC power supply; a drive unit for driving each of the semiconductor switching devices; a rectifier unit connected to a secondary winding of the leakage transformer; a magnetron connected to the rectifier unit; and a dead time generation circuit for turning off the semiconductor switching devices concurrently, wherein the drive unit has a function of limiting the lowest frequency of a frequency with which	in which the series circuit is connected to the direct current power supply in parallel, and, in an AC equivalent circuit, an end of the resonance circuit is connected to an intermediate point of one end of the series circuit and the other end is connected to an end of the direct current power supply, and further comprising, a drive means for driving the respective semiconductor switching elements; a rectifying means, which is connected to a secondary coil of the leakage transformer; and a magnetron, which is connected to the rectifying means, wherein a variable dead time preparation circuit which allows a period for which respective semiconductor switching elements are simultaneously turned off to vary in response to the switching frequency is provided.

the semiconductor switching devices are driven, so that the lowest frequency is set to be high at the beginning of operation of the high-frequency heating apparatus, and the lowest frequency is set to be lower gradually thereafter. Claim 2. A high-frequency heating apparatus for driving a magnetron, comprising: a DC power supply including an AC power supply, a rectifier circuit for rectifying a voltage of the AC power supply, and a smoothing capacitor for smoothing an output voltage of the rectifier circuit; two series circuits each including two semiconductor switching devices, each of the series circuits being connected in parallel to the AC power supply; a resonance circuit connected to a primary winding of a leakage transformer and a capacitor, one end of	Claim 2. A high frequency heating apparatus for driving a magnetron, comprising, a direct current power supply; two sets of series circuits each consisting of a pair of semiconductor switching elements; and a resonance circuit connected with a primary coil of a leakage transformer and a capacitor; in which two sets of the series circuits are respectively connected to the direct current power supply in parallel, and I0 an end of the resonance circuit is connected to an intermediate point of the one end of series circuits and the other end thereof is connected to an intermediate point of the other direct current power supply, and further comprising, a drive means for driving the respective semiconductor switching elements; a rectifying means, which is connected to a secondary coil

the resonance circuit being connected to a middle point of one of the series circuits while the other end of the resonance circuit is connected to a middle point of the other series circuit; a drive unit for driving each of the semiconductor switching devices; a rectifier unit connected to a secondary winding of the leakage transformer; a magnetron connected to the rectifier unit; and a dead time generation circuit for turning off the semiconductor switching devices concurrently, wherein the drive unit has a function of limiting the lowest frequency of a frequency with which the semiconductor switching devices are driven, so that the lowest frequency is set to be high at the beginning of operation of the high-frequency heating apparatus, and the lowest frequency is set to be lower gradually thereafter.	of the leakage transformer; and a magnetron, which is connected to the rectifying means, wherein a variable dead time preparation circuit which allows a period for which respective semiconductor switching elements are simultaneously turned off to vary in response to the switching frequency is provided. Claim 3. A high frequency heating apparatus for driving a magnetron, comprising, a direct current power supply; a series circuit consisting of a pair of semiconductor switching elements; and a resonance circuit connected with a primary coil of a leakage transformer and a capacitor; in which the series circuit is connected to the direct current power supply in parallel, and the resonance circuit is connected in parallel to one of the

Claim 3. A high-frequency heating apparatus for driving a magnetron, comprising: a DC power supply including an AC power supply, a rectifier circuit for rectifying a voltage of the AC power supply, and a smoothing capacitor for smoothing an output voltage of the rectifier circuit; a series circuit including two semiconductor switching devices, the series circuit being connected in parallel to the AC power supply; a resonance circuit connected to a primary winding of a leakage transformer and a capacitor, the resonance circuit being connected in parallel to one of the semiconductor switching devices; a drive unit for driving each of the semiconductor switching devices; a rectifier unit connected to a secondary winding of	semiconductor switching elements, and further comprising, a drive means for driving the respective semiconductor switching elements; a rectifying means, which is connected to a secondary coil of the leakage transformer; and a magnetron, which is connected to the rectifying means, wherein a variable dead time preparation circuit which allows a period for which respective semiconductor switching elements are simultaneously turned off to vary in response to the switching frequency is provided.

the leakage transformer; a magnetron connected to the rectifier unit; and a dead time generation circuit for turning off the semiconductor switching devices concurrently, wherein the drive unit has a function of limiting the lowest frequency of a frequency with which the semiconductor switching devices are driven, so that the lowest frequency is set to be high at the beginning of operation of the high-frequency heating apparatus, and the lowest frequency is set to be lower gradually thereafter.	

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to THIEN TRAN whose telephone number is (571)270-7745. The examiner can normally be reached on Mon-Thurs, 8-5PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoang Tu can be reached on (571)272-4780. The fax

phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. T./
Examiner, Art Unit 3742

/TU B HOANG/
Supervisory Patent Examiner, Art Unit 3742